

**REMARKS**

By this Amendment, Applicants have amended claims 1, 2, and 4-9 to place them in proper U.S. format, and canceled claim 13 without prejudice or disclaimer.

Claims 1-12 remain pending.

In the last Office Action, the Examiner:

- a. objected to claims 4-12 under 37 C.F.R. § 1.75(c) for being multiply dependent upon other multiple dependent claims;
- b. rejected claim 13 under 35 U.S.C. § 102(b) over U.S. Patent No. 5,347,513 ("*Abefelt*");
- c. rejected claims 1 and 3 under 35 U.S.C. § 103(a) over U.S. Patent No. 6,744,778 ("*Allpress*") and U.S. Patent No. 5,883,901 ("*Chiu*");
- d. rejected claims 2 and 4-7 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and *Abefelt*; and
- e. rejected claims 8-12 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and an IEEE article entitled "DTM: New Dynamic Transfer Mode using Dynamically Assigned Short-hold Time-slot Relay" ("*Yamanaka*").

***OBJECTION UNDER 37 C.F.R. § 1.75(c)***

Applicants have amended claims 4-9 to depend only upon claim 1. Accordingly, the objection to claims 4-12 under 37 C.F.R. § 1.75(c) for being multiply dependent upon other multiple dependent claims is deemed overcome.

### **REJECTION OF CLAIM 13**

Applicants respectfully traverse the rejection of claim 13 under 35 U.S.C. § 102(b) over *Abefelt*. However, in the interest of advancing the prosecution of the present application, Applicants have canceled claim 13 without prejudice or disclaimer of the subject matter contained therein. Applicants reserve the right to pursue the subject matter in claim 13 at a later time in the present application or another application, such as a continuing application.

### **REJECTION OF CLAIMS 1 AND 3**

Applicants respectfully traverse the rejection of claim 1 under 35 U.S.C. § 103(a) over *Allpress* and *Chiu* because no prima facie case of obviousness has been established. No prima facie case of obviousness has been established at least for the reason that the cited art fails to teach or suggest, separately or in combination, each and every element in claim 1. For example, *Allpress* and *Chiu* fail to teach or suggest, separately or in combination, at least “associating . . . time slots which define channels conveying payload traffic with a respective additional bit . . . indicating whether control information exists regarding the time slot associated with the respective additional bit” and “conveying said control information . . . as at least some of the n bits of the time slot associated with said additional bit,” as recited in claim 1.

In contrast, *Allpress* merely discloses a time division multiple access communication system where downlink data are transmitted over a data channel in repeated time frames, each frame containing a plurality of time slots. *Allpress*, col. 1, lines 50-54. Control data are transmitted over a dedicated physical control channel (DPCCH) and data information is transmitted over a dedicated physical data channel

(DPDCH). *Id.*, Fig. 1; col. 2, lines 41-59. The DPCCH and DPDCH form a downlink dedicated transmission channel. *Id.* Each frame on the channel includes a user packet flag (UPF) in the DPDCH, that indicates whether or not each time slot of the DPDCH in the frame contains data. *Id.*, Fig. 1; col. 3, lines 4-6. The UPF is composed of several fields, where each field indicates the status of a corresponding slot of the DPDCH whether or not there is a packet for specific user. *Id.*, Fig. 1; col. 3, lines 1-10. Each slot of the dedicated transmission channel includes control information, even when there is no user data in the DPDCH, and this control information is transmitted over the DPCCH, not the DPDCH. *Id.*, col. 3, lines 32-37. That is, this control information is transmitted in time slots of the DPCCH, which is not associated with the UPF because the UPF refers to slots of the DPDCH. Hence, the UPF disclosed in *Allpress* does not teach or suggest “a respective additional bit . . . indicating whether control information exists regarding the time slot associated with the respective additional bit” and “conveying said control information . . . as at least some of the n bits of the time slot associated with said additional bit,” as recited in claim 1.

Further, *Chiu* fails to cure the deficiencies of *Allpress*. *Chiu* merely discloses conveying data in frames, where a number of frames form a time slot. *Chiu*, col. 13, line 65 to col. 14, line 47; col. 7, lines 66-67. In *Chiu*, there are two types of payload frames: ones that carry subscriber data and ones that carry modem control messages. *Id.*, col. 14, lines 15-17. A one-bit flag indicates whether the frame has subscriber data or a modem control message. *Id.*, col. 14, line 17-18. Hence, the one-bit flag disclosed in *Chiu* does not teach or suggest “associating . . . time slots (110A) which define channels conveying payload traffic with a respective additional bit . . . indicating whether

control information exists regarding the time slot associated with the respective additional bit” and “conveying said control information . . . as at least some of the n bits of the time slot associated with said additional bit,” as recited in claim 1.

Accordingly, for at least the reason that *Allpress* and *Chiu* fail to teach or suggest, separately or in combination, each and every element in claim 1, no prima facie case of obviousness has been established. Thus, the rejection of claim 1 under 35 U.S.C. § 103(a) over those references should be withdrawn, and claim 1 should be allowed.

Applicants respectfully traverse the rejection of claim 3 under 35 U.S.C. § 103(a) over *Allpress* and *Chiu*. Claim 3 depends upon allowable claim 1, and includes all limitations in claim 1. Accordingly, the rejection of claim 3 under 35 U.S.C. § 103(a) over *Allpress* and *Chiu* should be withdrawn for at least the reasons discussed above for claim 1, in addition to the patentable subject matter recited in claim 3.

#### **REJECTION OF CLAIMS 2 AND 4-7**

Applicants respectfully traverse the rejection of claims 2 and 4-7 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and *Abefelt* because no prima facie case of obviousness has been established. Claims 2 and 4-7 depend upon claim 1, and include all limitations in claim 1. As discussed above, no prima facie case of obviousness has been established with respect to claim 1, for at least the reason that *Allpress* and *Chiu* fail to teach or suggest every limitation in claim 1. With respect to claim 1, *Abefelt* fails to cure the deficiencies of *Allpress* and *Chiu*.

Specifically, *Abefelt* merely discloses a fast-operating packet and circuit switch combination. *Abefelt*, Abstract. The switch establishes connections between a plurality

of units that are distributed locally within a system and mutually connected by physical links. *Id.*, col. 1, lines 7-10. However, *Abefelt* does not teach or suggest at least “associating . . . time slots which define channels conveying payload traffic with a respective additional bit . . . indicating whether control information exists regarding the time slot associated with the respective additional bit” and “conveying said control information . . . as at least some of the n bits of the time slot associated with said additional bit,” as recited in claim 1.

Accordingly, for at least the reason that *Allpress*, *Chiu*, and *Abefelt* fail to teach or suggest, separately or in combination, each and every element in claim 1, no prima facie case of obviousness has been established. Thus, the rejection of claims 2 and 4-7 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and *Abefelt* should be withdrawn at least because no prima facie case of obviousness has been established for their base claim (i.e., claim 1).

#### **REJECTION OF CLAIMS 8-12**

Applicants respectfully traverse the rejection of claims 8-12 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and *Yamanaka*. Claims 8-12 depend upon claim 1, and include all limitations in claim 1. As discussed above, no prima facie case of obviousness has been established with respect to claim 1, for at least the reason that *Allpress* and *Chiu* fail to teach or suggest every limitation in claim 1. With respect to claim 1, *Yamanaka* fails to cure the deficiencies of *Allpress* and *Chiu*.

Specifically, *Yamanaka* merely discloses a network architecture called Dynamic Transfer Mode (DTM). *Yamanaka*, Abstract. In a DTM network, a connection is set up on-the-fly by sending a series of routing link identifiers to a destination, such that burst

data transfers are more efficiently carried. *Id.* However, *Yamanaka* does not teach or suggest at least “associating . . . time slots (110A) which define channels conveying payload traffic with a respective additional bit . . . indicating whether control information exists regarding the time slot associated with the respective additional bit” and “conveying said control information . . . as at least some of the n bits of the time slot associated with said additional bit,” as recited in claim 1.

Accordingly, for at least the reason that *Allpress*, *Chiu*, and *Abefelt* fail to teach or suggest, separately or in combination, each and every element in claim 1, no prima facie case of obviousness has been established. Thus, the rejection of claims 8-12 under 35 U.S.C. § 103(a) over *Allpress*, *Chiu*, and *Yamanaka* should be withdrawn at least because no prima facie case of obviousness has been established for their base claim (i.e., claim 1).

### **CONCLUSION**

Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

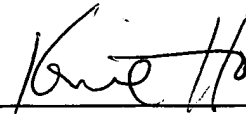
Further, Applicants note that the Office Action contains numerous statements reflecting apparent assertions concerning the related art and claims. Regardless of whether any such statement is specifically addressed herein, Applicants decline to automatically subscribe to any assertion and/or characterization set forth in the Office Action.

Please grant any extensions of time required to enter this response and charge  
any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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